UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/683,641	10/09/2003	Dwight W. Mattix	030393	1207

23696 7590 08/09/2006

QUALCOMM INCORPORATED
5775 MOREHOUSE DR.
SAN DIEGO, CA 92121

EXAMINER	
NORRIS, JEREMY C	

ART UNIT	PAPER NUMBER
2841	

DATE MAILED: 08/09/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/683,641	MATTIX, DWIGHT W.	
	Examiner	Art Unit	
	Jeremy C. Norris	2841	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 May 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21 and 23-57* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21,23-57* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 May 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

The drawings were received on 17 May 2006. These drawings are acceptable.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-6, 8, 9, 21, 23, 26-35, 37-42, 44-49, and 51-57 are rejected under 35 U.S.C. 102(b) as being anticipated by US 6,329,610 (Takubo).

Takubo discloses, referring primarily to figure 17, an interlayer interconnection unit for a printed circuit board (PCB), comprising: an interstitial bridge pad (106a) having a first side (top side as viewed in figure 17) and a second side (bottom side as viewed in figure 17), wherein said first side of said interstitial bridge pad physically contacts a first dielectric layer (103) and said second side of said interstitial bridge pad physically contacts a second dielectric layer (101); a first blind via (107b) disposed on said first side of said interstitial bridge pad, wherein said first blind via extends through said first dielectric layer and a second blind via (shown not referenced) disposed on said second side of said interstitial bridge pad, wherein said second blind via extends through said second dielectric layer, wherein said interstitial bridge pad is adapted to electrically connect said first blind via to said second blind via [claim 1], wherein said interstitial

bridge pad comprises a disc-shaped conductive element (col. 26, lines 55-65) [claim 2] wherein said first blind via extends from a first conductive layer (104b), through said first dielectric layer, and to said first side of said interstitial bridge pad, and said second blind via extends from a second conductive layer (106b), through said second dielectric layer; and to said second side of said interstitial bridge pad [claim 3], wherein said first conductive layer and said second conductive layer each comprise copper foil (col. 15, lines 45-55) [claim 4], wherein said first blind via extends from a first capture pad (104b) to said first side of said interstitial bridge pad, and said second blind via extends from a second capture pad (106b) to said second side of said interstitial bridge pad [claim 5], wherein said first capture pad and said second capture pad each have a diameter less than a diameter of said interstitial bridge pad [claim 6], wherein: said PCB comprises a bridge layer disposed between said first dielectric layer and said second dielectric layer, and said interstitial bridge pad is located within said bridge layer, and wherein said interstitial bridge pad lacks electrical connection, within said bridge layer, to a conductive element of said bridge layer [claim 8], wherein said interstitial bridge pad is coaxial in a z direction with said first blind via and with said second blind via [claim 9].

Also, Takubo discloses, a carrier for a multilayer printed circuit board (PCB), said carrier comprising a pseudo three-layer core, said pseudo three-layer core including: a first metal layer (106b); a first dielectric layer (101) disposed on said first metal layer; a bridge layer (106a) disposed on said first dielectric layer; a second dielectric layer (103) disposed on said bridge layer; and a second metal layer (104b) disposed on said second dielectric layer, wherein said bridge layer comprises a plurality of spaced apart

interstitial bridge pads, and wherein at least one of said plurality of interstitial bridge pads is adapted for providing an interlayer interconnection between said first metal layer and said second metal layer, and wherein each of said plurality of interstitial bridge pads is physically connected to said first metal layer by a first blind via transversing said first dielectric layer, and wherein each of said plurality of interstitial bridge pads is physically connected to said second metal layer by a second blind via transversing said second dielectric layer [claim 21], wherein said bridge layer lacks an electrical connection between said plurality of interstitial bridge pads [claim 23], wherein said first metal layer comprises a first signal layer of said PCB, and said second metal layer comprises a second signal layer of said PCB [claim 26], further comprising at least a third signal layer (104b) laminated to said pseudo three-layer core [claim 27], wherein said carrier comprises from 2 to 4 additional layers (104b, 104a) laminated to said pseudo three-layer core [claim 28].

Moreover, Takubo discloses, a pseudo three-layer core for a printed circuit board (PCB), comprising: a plurality of interlayer interconnection units, wherein each of said plurality of interlayer interconnection units extends from a first metal layer (106b) to a second metal layer (104b); a first dielectric layer (101) disposed on said first metal layer; a bridge layer (106a) disposed on said first dielectric layer; and a second dielectric layer (103) disposed on said bridge layer, wherein said second metal layer is disposed on said second dielectric layer, and wherein at least one of said plurality of interlayer interconnection units comprises: an interstitial bridge pad located within said bridge layer; a first blind via (shown not referenced) extending from said first metal layer to a

first side of said interstitial bridge pad; and. a second blind via (107b) extending from said second metal layer to a second side of said interstitial bridge pad [claim 29]

Furthermore, Takubo discloses a multi-layer printed circuit board (PCB), comprising: a first signal layer (106a); a second signal layer (104a) a bridge layer (104b) disposed between said first signal layer and said second signal layer; and a plurality of interlayer interconnection units, each of said plurality of interlayer interconnection units adapted for connecting said first signal layer with said second signal layer through said bridge layer, wherein at least one said plurality of interlayer interconnection units comprises: a pair of opposed coaxial blind vias (107b, and another shown not referenced) transversing a first dielectric layer and a second dielectric layer; and a bridge pad (104b) physically contacting said first and second dielectric layers, said bridge pad in electrical contact with said pair of blind vias [claim 30], wherein: said bridge pad includes a first side and a second side; and wherein said pair of opposed coaxial blind vias comprise a first blind via disposed on said first side of said bridge pad, and a second blind via disposed on said second side of said bridge pad [claim 31], further comprising at least one additional dielectric layer (101) laminated to said first signal layer, and at least one additional signal layer (106b) laminated to said at least one additional dielectric layer [claim 32].

Moreover, Takubo discloses, a multi-layer PCB, comprising: at least one pseudo three-layer core including: a first metal layer (106b); a first dielectric layer (101) disposed on said first metal layer; a bridge layer (106a) disposed on said first dielectric layer; a second dielectric layer (103) disposed on said bridge layer; a second metal

layer (104b) disposed on said second dielectric layer; and a plurality of interlayer interconnection units for electrically interconnecting said first metal layer with said second metal layer, wherein at least one of said plurality of interlayer interconnection units comprises: an interstitial bridge pad (106a) having a first side and a second side; a first blind via (shown not referenced) disposed on said first side of said interstitial bridge pad and a second blind via (107b) disposed on said second side of said bridge pad [claim 33], wherein each of said plurality of interlayer interconnection units is adapted for electrically interconnecting said first metal layer with said second metal layer [claim 34], wherein each of said first metal layer and said second metal layer comprises a signal layer and said multilayer PCB further .comprises at least one additional signal layer (104a) laminated to said at least one pseudo three-layer core [claim 35], wherein said multilayer PCB comprises from 1 to 4 pseudo three-layer cores and from 4 to 28 signal layers [claim 37].

Additionally, Takubo discloses, a multilayer PCB, comprising: means for carrying a plurality of signal layers; and means for interconnecting at least two of said plurality of signal layers, wherein said carrying means comprises a pseudo three-layer core, wherein said pseudo three-layer core includes an internal bridge layer (106a) that comprises a plurality of interstitial bridge pads, a first dielectric layer (101), and a second dielectric layer (103) and wherein said interconnecting means comprises a pair of opposed blind vias disposed on either side of each of said plurality of interstitial bridge pads said pair of opposed blind vias transversing said first and second dielectric layers [claim 38], wherein said bridge layer comprises an internal pseudo metal layer

(106a) disposed between a first dielectric layer (101) and a second dielectric layer (103), and wherein said interconnecting means is adapted for interconnecting said plurality of signal layers [claim 39].

In addition, Takubo discloses a method for forming a multilayer printed circuit board (PCB), comprising: a) providing a metal clad first dielectric layer (101) having first metal clad side and a second metal clad side, b) forming a bridge layer (106a) from said second metal clad side, wherein said bridge layer comprises a plurality of bridge pads disposed on said first dielectric layer, and wherein said first metal clad side comprises a first metal layer (106b); c) providing a second dielectric layer (103) on said bridge layer, wherein said second dielectric layer has a second metal layer (104b) disposed thereon; d) forming a first blind via through said first dielectric layer (shown not referenced), wherein said first blind via extends from said first metal layer to a first side of at least one of said plurality of bridge pads; and e) forming a second blind via (107b) through said second dielectric layer, wherein said second blind via extends from said second metal layer to a second side of said at least one of said plurality of bridge pads [claim 40], wherein said step b) comprises etching said second metal clad side of said first dielectric layer to form said at least one of said plurality of bridge pads (col. 21, lines 10-15) [claim 41], wherein: said second metal clad side comprises copper foil, and wherein said at least one of said plurality of bridge pads comprises copper (col. 21, lines 10-15) [claim 42], wherein said bridge layer lacks electrical connectivity between said plurality of bridge pads [claim 44], wherein said steps c) and d) respectively comprise forming said first blind via and said second blind via by a process selected from the group

consisting of laser drilling, plasma drilling, and photo-defining (col. 22, lines 5-25) [claim 45], further comprising: e) plating shut said first blind via and said second blind via (col. 26, lines 55-65) [claim 46], wherein said method involves only a single plating cycle [claim 47], wherein after said step e), said first metal layer and said second metal layer each have a thickness in the range of from about 0.8 to 1.4 mils (col. 22, lines 10-15) [claim 48], wherein after said step e) said first metal layer and said second metal layer each have a thickness in the range of from about 0.9 to 1.1 mils (col. 22, lines 10-15) [claim 49].

Moreover, Takubo discloses, a method for forming a multilayer printed circuited board (PCB), comprising: a) forming a pseudo three-layer core, said pseudo three-layer core including: a first metal layer (106b); a first dielectric layer (101) disposed on said first metal layer, a bridge layer (106a) disposed on said first dielectric layer; a second dielectric layer (103) disposed on said bridge layer; and a second metal layer (104b) disposed on said second dielectric layer, wherein said bridge layer comprises a plurality of spaced apart interstitial bridge pads; and b) forming a plurality of interlayer interconnection units for interconnecting said first metal layer and said second metal layer, wherein each of said interlayer interconnection units includes: a first blind via (shown not referenced) disposed on a first side of one of said plurality of interstitial bridge pads, wherein said first blind via extends from said first metal layer through said first dielectric layer; and a second blind via disposed on a second side of one of said plurality of interstitial bridge pads, wherein said second blind via (107b) extends from said second metal layer through said second dielectric layer [claim 51], wherein: said

step b) comprises plating shut said first blind via and said second blind via, and said method includes only a single plating cycle (col. 26, lines 55-65) [claim 52], wherein each of said first blind via and said second blind via has an aspect ratio of at least about 1:1 [claim 53], wherein each of said interlayer interconnection units has an effective aspect ratio of at least about 2:1 [claim 54].

Alternately, Takubo discloses, referring primarily to figure 2, a method for forming a multilayer printed circuit board (PCB), comprising: a) a step for forming a pseudo three-layer core, wherein said pseudo three- layer core includes a first metal layer (12a), a first dielectric layer (21c) disposed on said first metal layer; a bridge layer (16) disposed on said first dielectric layer; a second dielectric layer (21b) disposed on said bridge layer; and a second metal layer (15) disposed on said second dielectric layer; and b) a step for forming a plurality of interlayer interconnection units for electrically interconnecting said first metal layer and said second metal layer, wherein each of said interlayer interconnection units includes a pair of opposed coaxial blind vias (31), and a bridge pad disposed between, and in electrical contact with, said pair of blind vias, wherein said bridge layer comprises a plurality of said bridge pads [claim 55].

Similarly, Takubo discloses method for forming a pseudo three-layer core for a PCB, comprising: a) providing a first metal layer (12a), b) providing a first dielectric layer (21c) on said first metal layer; c) forming a bridge layer (16) on said first dielectric layer, said bridge layer comprising a plurality of bridge pads; d) providing a second dielectric layer (21b) on said bridge layer; e) providing a second metal layer on said second dielectric layer; f) forming a first blind via (31) on a first side of each of said plurality of

bridge pads, wherein said first blind via extends from said first metal layer through said first P dielectric layer; and g) forming a second blind via (31) on a second side of each of said plurality of bridge pads, wherein said second blind via extends from said second metal layer through said second dielectric layer [claim 56], wherein: said first dielectric layer comprises a first side and a second side, said first side having said first metal layer disposed thereon, and said second side having a layer of copper foil disposed thereon, and said step c) comprises etching said layer of copper foil (col. 22, lines 10-20) [claim 57].

Claims 10-12 and 14-18 are rejected under 35 U.S.C. 102(b) as being anticipated by US 2001/0020548 A1 (Burgess).

Burgess discloses, referring primarily to figure 26, an interlayer interconnection unit for a multi-layer PCB, comprising: a first capture pad (shown not referenced, part of layer 2) having a first annular ring; a first via (113') having a first via inner end and a first via outer end, said first via outer end in contact with said first capture pad and encircled by said first annular ring; an interstitial bridge pad (shown not referenced, part of layer 53) having a first side and a second side, said first via inner end in contact with said first side of said interstitial bridge pad; a second via (50) having a second via inner end and a second via outer end, said second via inner end in contact with said second side of said interstitial bridge pad; and a second capture pad (shown not referenced, part of layer 4) having a second annular ring, said second via outer end in contact with said second capture pad and encircled by said second annular ring, wherein a first interstitial

bridge pad of said at least one interstitial bridge pad lacks electrical connectivity to others of said at least one interstitial bridge pads (as shown in figure 26, there is only one such interstitial bridge pad, thus, said pad is not electrically connected to any other such bridge pad) [claim 10], wherein said first annular ring, said first via, said interstitial bridge pad, said second via and said second annular ring are coaxial with each other [claim 11], wherein said first via extends through a first dielectric layer (51), and said second via extends through a second dielectric layer (52) [claim 12], wherein said multilayer PCB comprises an internal bridge layer (53), and said interstitial bridge pad is a component of said bridge layer [claim 14], wherein each of said first via and said , second via has an aspect ratio of at least about 1:1 [claim 15], wherein said interconnection unit has an effective aspect ratio greater, than about 2:1 [claim 16], wherein: said first capture pad is located within a first conductive layer (2) said second capture pad is located within a second conductive layer (4), and said interconnection unit further comprises a third via extending from said first capture pad or said second capture pad to a third conductive layer (1) [claim 17]

Similarly, Burgess discloses, a dual blind via interconnection unit for a multilayer PCB, comprising: a pair of opposed coaxial blind vias (50, 113') transversing a pair of dielectric layers (51, 52); and at least one bridge pad (shown not reference, part of layer 53) disposed between said pair of dielectric layers, wherein each of said pair of blind vias is in contact with said bridge pad and wherein said bridge pad is adapted to electrically interconnect said pair of opposed coaxial blind vias, wherein a first bridge pad of said at least one bridge pad lacks electrical connectivity to others of said at least

one bridge pads (as shown in figure 26, there is only one such interstitial bridge pad, thus, said pad is not electrically connected to any other such bridge pad) [claim 18].

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 7, 43, and 50 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takubo in view of US 2002/0117761 A1 (Zohni).

Takubo discloses the claimed invention as described above except Takubo does not specifically state that said interstitial bridge pad has a diameter in the range of from about 12 to 20 mils [claims 7, 43], wherein said first blind via and said second blind via each comprise a via having a diameter in the range of from about 4 to 5 mils [claim 50]. However, it is well known in the art to form pads and vias with diameters in the claimed ranges as evidenced by Zohni ([0023]). Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to form the pad an via diameters in

the invention of Takubo in the above stated ranges as is known in the art and evidenced by Zohni. The motivation for doing so would have been to produce a device with a high wiring density.

Claims 13, 19, and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Burgess in view of Zohni.

Burgess discloses the claimed invention as described above except Burgess does not specifically state that said interstitial bridge pad has a diameter in the range of from about 14 to 17 mils [claim 13], wherein said bridge pad has a diam' eter .. in the range of from about 12 to 20 mils [claim 19], wherein said first blind via and said second blind via each comprise a via having a diameter in the range of from about 4 to 6 mils [claim 20]. However, it is well known in the art to form pads and vias with diameters in the claimed ranges as evidenced by Zohni ([0023]). Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to form the pad an via diameters in the invention of Burgess in the above stated ranges as is known in the art and evidenced by Zohni. The motivation for doing so would have been to produce a device with a high wiring density. Moreover, it has been held that where the general conditions of a claim are disclosed in the prior art, discovering that optimum or workable ranges involves only routing skill in the art. *In re Aller,* 105 USPQ 233.

Claims 24 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takubo in view of US 5,928,005 (Li)

Takubo discloses the claimed invention as described above except Takubo does not specifically state that said plurality of interstitial bridge pads are spaced apart from each other by a distance in the range of from about 0.7 to 4 mils [claim 24], wherein said plurality of interstitial bridge pads are arranged within said bridge layer at a center-to-center pitch in the range of from about 15 to 25 mils [claim 25]. However, it is well known in the art to form pads with spacing in the claimed ranges as evidenced by Li (col. 10, lines 60-65). Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to form the pads in the invention of Takubo with spacing in the above stated ranges as is known in the art and evidenced by Li. The motivation for doing so would have been to produce a device with a high wiring density. Moreover, it has been held that where the general conditions of a claim are disclosed in the prior art, discovering that optimum or workable ranges involves only routing skill in the art. *In re Aller,* 105 USPQ 233.

Claim 36 is rejected under 35 U.S.C. 103(a) as being unpatentable over Takubo.

Takubo discloses the claimed invention as described above except Takubo does not specifically state that said at least one pseudo three- layer core comprises a first pseudo three-layer core and at least a second pseudo three-layer core laminated to said first pseudo three-layer core [claim 36]. However, the ordinarily skilled artisan would recognize that such a modification would only involved a mere duplication of the board explicitly disclosed by Takubo. Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to laminate a second three layer

board to the three layer board in the invention of Takubo. The motivation for doing so would have been to provide additional signal layers. Moreover, it has been held that mere duplication of the essential working parts of a device involves only routine skill in the art. *St. Regis Paper Co. v. Bemis Co.,* 193 USPQ 8.

Response to Arguments

Applicant's arguments filed 17 May 2006 have been fully considered but they are not persuasive. Applicant alleges "Takubo fails to teach or fairly suggest a structure having a bridge pad that 'physically contacts' two dielectric layers wherein each of the dielectric layers has a blind via 'transversing' therethrough". However, as clearly displayed in figure 17, the pad (106a) is in physical contact with two dielectric layers (101, 103) wherein the dielectric layers each have a blind via (one not specifically referenced, the other 107b) transversing therethrough. Additionally, regarding Burgess, Applicant alleges that Burgess fails to show the limitation "that at least one 'bridge pad lacks electrical connectivity' to any other bridge pads". However, Burgess only displays one such bridge pad, thus, Burgess does indeed disclose a bridge pad which lacks electrical connectivity to any other bridge pad. Thus, having addressed each of Applicant's arguments, the traversal of the rejection on these grounds is deemed unsuccessful.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeremy C. Norris whose telephone number is 571-272-1932. The examiner can normally be reached on Monday - Friday, 9:30 am - 5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamand Cuneo can be reached on 571-272-1957. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

JCSN

KAMAND CUNEO
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800